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L8	((mult$3 adj frequenc$3) or (multifrequenc$3)) same ((pll) or (phase adj lock$3 adj loop) or (phase adj lock$3)) same (frequenc$3 near2 select$3)	11	L8
L7	((wide$3 adj frequenc$3) or (widefrequenc$3)) same ((pll) or (phase adj lock$3 adj loop) or (phase adj lock$3)) same (frequenc$3 near2 select$3)	11	L7
L6	((wide$3 adj channel$) or (widechannel$)) same ((pll) or (phase adj lock$3 adj loop) or (phase adj lock$3)) same (channel$ near2 select$3)	2	L6
L5	((multi$3 adj channel$) or (multichannel$)) same ((pll) or (phase adj lock$3 adj loop) or (phase adj lock$3)) same (channel$ near2 select$3)	24	L5
L4	((wide adj band$) or (wideband)) same ((pll) or (phase adj lock$3 adj loop) or (phase adj lock$3)) same (band$ near2 select$3)	31	L4
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DOCUMENT-IDENTIFIER: US 4201945 A
TITLE: Phase comparing apparatus

Detailed Description Text (12):
Now a lock detecting circuit for a phase locked loop employed in a multiband radio receiver will be described in the following. Considering a case of a radio receiver of two bands switchable between AM and FM bands, it is preferred that the frequency of the reference frequency signal .theta.R for phase comparison should also be changed in association with the difference of the local oscillation frequencies in both bands. More specifically, since the local oscillation frequency in the FM band is high, it is preferred that the frequency of the reference signal .theta.R for phase comparison be also selected to be high for precise phase comparison. Thus, in case where the frequency of the difference signal .theta.R for a phase comparison is changed in association with selection of the bands, it is necessary to change the detection sensitivity of the phase difference in association with the bands.

Detailed Description Text (16):
FIG. 10 shows a block diagram of such a lock detecting circuit of a phase locked loop for use in a multiband radio receiver. Referring to FIG. 10, the frequency division rate of the frequency dividers 2 and 2' and the resistance values of the MOS transistors 18 and 18' when the same are in conduction are selected to be different and either frequency divider and either MOS transistor are selected through control of gates 28, 29, 30 and 31 responsive to the output of a band switching circuit 27. Although the FIG. 10 embodiment has been structured such that the detection sensitivity, i.e. the discharging time constant of the capacitor is changed in association with the band through selection of the MOS transistors that have different conduction resistance values, alternatively the embodiment may be structured such that capacitors having different capacitance values are selected responsive to band switching. The embodiment is also shown comprising a circuit 26 for providing a pickup signal of the fall of the frequency signal .theta.R, which may be implemented by inverters and a NOR gate, as shown in FIG. 8.

L9: Entry 55 of 88 File: USPT Mar 18, 1980

DOCUMENT-IDENTIFIER: US 4194151 A
TITLE: Multifrequency generator

Abstract Text (1):
A multifrequency generator is provided for a radio transmitter and receiver that must operate on a plurality of channels. The generator includes a channel synthesizer having a phase-locked loop that provides a respective output frequency signal for each selected channel. The generator includes a transmitter synthesizer connected to the channel synthesizer and having a phase-locked loop and a mixer that provide the transmitter synthesizer output signal. The generator includes a receiver synthesizer connected to the channel synthesizer and having a phase-locked loop and a mixer that provide the receiver synthesizer output signal. The frequency of the channel synthesizer output frequency is selected to be substantially lower than the transmitter and receiver synthesizer output frequencies to reduce the noise sideband components of the transmitter and receiver output signals.

Brief Summary Text (13):
Briefly, these and other objects are achieved in accordance with our invention by a multifrequency generator having a channel synthesizer, a transmitter synthesizer, and a receiver synthesizer. The channel synthesizer comprises a reference oscillator and a voltage-controlled oscillator connected in a phase-locked loop to provide a selectable chanel frequency. The channel frequency is applied to the transmitter synthesizer which comprises a modulated reference oscillator, a voltage-controlled oscillator, and a mixer connected in a phase-locked loop. The transmitter synthesizer output frequency is mixed with the reference frequency, and the difference between the two mixed frequencies and the selected channel frequency are used to control the transmitter synthesizer output frequency. For a separate receiver frequency, the channel frequency is applied to the receiver synthesizer which comprises a reference oscillator, a voltage-controlled oscillator, and a mixer connected in a phase-locked loop. The receiver synthesizer output frequency is mixed with the reference frequency, and the difference between the two mixed frequencies and the selected channel frequency are used to control the receiver synthesizer output frequency. Thus, a plurality of selectable frequency signals can be provided with a minimum or relatively small number of reference frequency oscillators.

L9: Entry 51 of 88 File: USPT Nov 24, 1981

DOCUMENT-IDENTIFIER: US 4302845 A
TITLE: Phase-encoded data signal demodulator

Detailed Description Text (8):
Each pulse output signal from monostable 150 clocks the state of the complemented data clock into phase comparing flip-flop 158. The Q output of phase comparing flip-flop 128 is coupled to up/down counter 126 for controlling whether counter 126 counts up or down at the 80 KHz data clock signal frequency. If the Q output of phase comparing flip-flop 128 has a logical one state, counter 126 will count up until it reaches a preselected state that is detected by overflow decoding circuitry 122, which causes by way of flip-flop 121 the addition of a .phi..sub.2 clock pulse for appropriately adjusting the phase of the 10 KHz data clock signal. Similarly, if the Q output of phase comparing flip-flop 128 has a logical zero state, counter 126 counts down until a preselected state is detected by underflow decoding circuitry 124, which causes by way of flip-flop 123 a .phi..sub.1 clock pulse to be deleted for appropriately adjusting the phase of the 10 KHz data clock signal. Both the outputs from flip-flops 121 and 124 are coupled by way of OR gate 130 for resetting counter 126 to a predetermined initial state. The rate at which phase adjustments are made to the 10 KHz data clock signal is determined by the preselected states that are decoded by overflow decoding circuitry 122 and underflow decoding circuitry 124. The rate at which phase adjustments are made can be changed by varying the state at which an overflow or underflow is detected by means of the bandwidth select signal. If narrow bandwidth operation is desired, a first state of the bandwidth select signal may provide that overflow and underflow conditions are detected at a state representative of a relatively high totalized count. Conversely, if wide bandwidth operation is desired, a second state of the bandwidth select signal may provide that overflow and underflow conditions are detected at a state representative of a relatively low totalized count. By utilizing the bandwidth select signal, the rate at which digital phase-locked loop 160 locks to the bit transitions of the phase-encoded data signal may be adjusted up or down depending on the format of the data signal and the characteristics of the particular communication channel utilized.

L9: Entry 14 of 88 File: USPT Oct 5, 1999

DOCUMENT-IDENTIFIER: US 5963068 A
TITLE: Fast start-up processor clock generation method and system

Detailed Description Text (3):
With reference now to the figures, and in particular with reference to FIG. 1, there is shown a conventional microcontroller system having a PLL based clock generation circuit. A microcontroller based system 100 includes a dual bandwidth PLL clock generation circuit 105. A dual bandwidth PLL is used in systems requiring a fast startup time but having a low frequency input reference to the PLL, for example. A dual bandwidth PLL has two phases of operation: 1) a wide bandwidth (high gain) phase and 2) a narrow bandwidth (low gain) phase. As used in power conscious designs, a low frequency reference clock (REF) is input into PLL 110 within circuit 105, which synthesizes the reference clock to produce the PLL circuit output (PLL CLOCK) as a function of a multiplication factor input (N). In some systems, PLL 110 is a dual bandwidth PLL to decrease lock time. PLL 110 outputs the PLL CLOCK to a divider 130 and outputs a FREQUENCY Lock signal to a counter 120. The FREQUENCY LOCK signal indicates when the PLL clock has reached the programmed frequency of the PLL to within a selected bandwidth, while the PLL is operating in a wide bandwidth mode. However, because the PLL must still reach a phase locked condition before the PLL can switch from the wide bandwidth to narrow bandwidth operation, an empirically derived settling time, for example 10 milliseconds, is counted off by counter 120 to ensure that the PLL has phase-locked. After the 10 milliseconds has been counted, counter 120 outputs a PHASE LOCK signal to CPU 140 to allow CPU 140 to begin execution while being clocked by the system clock (SYSTEM CLOCK).

Detailed Description Text (8):
PLL 310 also outputs a FREQUENCY LOCK signal to a counter 320 and CPU 350. The FREQUENCY LOCK signal indicates when the PLL CLOCK has reached the programmed output frequency of the CLOCK GENERATION CIRCUIT to within a selected bandwidth. However, because the PLL must still reach a phase locked condition to allow the PLL to switch from the wide bandwidth to narrow bandwidth operation and reach a stable frequency, a settling period indicated by a PHASE LOCK signal is counted off by counter 320 to ensure that the PLL has phase-locked. The FREQUENCY LOCK signal initiates the target frequency enable counter 320 to count off the preset period from t.sub.1 to t.sub.2. Counter 320 generates the PHASE LOCK signal input into AND gate 340 at the end of the count. The FREQUENCY LOCK signal also enables CPU 350 to begin operation and perform programmed tasks during the phase locking period. Because the processor is being clocked by SYSTEM CLOCK at a divided frequency, there is no danger of exceeding the maximum specified frequency during the phase/frequency lock period.

L9: Entry 26 of 88 File: USPT Oct 23, 1990

DOCUMENT-IDENTIFIER: US 4965534 A
TITLE: Channel frequency generator for use with a multi-frequency output generator

Brief Summary Text (2):
The present invention generally relates to a channel frequency generator for use with a multi-frequency output generator and, more particularly, to a microprocessor controlled cable television channel frequency generator which phase locks a frequency-agile modulated output to the same frequency as that of any selected channel of a comb generated output.

Brief Summary Text (15):
In accordance with the present invention, a channel frequency generator for use with a multi-frequency output generator is provided to which uses a phase lock loop responsive to selected outputs of the multi-frequency output generator, to provide a frequency coherent output at a selected frequency by modulating an input signal at a predetermined frequency spacing with respect to the selected frequency.

L9: Entry 33 of 88 File: USPT Apr 21, 1987

DOCUMENT-IDENTIFIER: US 4660182 A
TITLE: Programmable multichannel sonobuoy transmitter

Brief Summary Text (9):
Briefly, these and other objects of the present invention are accomplished by a programmable multichannel sonobuoy transmitter including a phase-locked loop which is modulated in order to transmit acquired acoustic data. Within the loop, a VCO (voltage-controlled oscillator) receives a modulation signal through a compensation network that corrects for the roll-off characteristic of the loop's response, and an independent tuning signal to generate an output frequency. A programmable counter/divider divides this frequency by a factor N corresponding to the selected channel, and the output thereof is compared in a phase detector with a reference frequency generated by a crystal oscillator. If the divided and reference frequencies differ in phase, an error voltage is generated at the phase detector and modified by a filter into a ramp voltage with the proper loop response. The ramp voltage is subsequently applied to the VCO as the tuning signal to change the output frequency in a direction which decreases the error voltage until phase lock occurs and the output frequency is stabilized. When another channel is desired, the corresponding factor N is changed in the counter/divider, and a new error voltage generated until the loop locks on the new output frequency.

L9: Entry 7 of 88 File: USPT Apr 10, 2001

DOCUMENT-IDENTIFIER: US 6215834 B1
TITLE: Dual bandwidth phase locked loop frequency lock detection system and method

Detailed Description Text (12):
While the invention has been described in the context of a preferred embodiment, it will be apparent to those skilled in the art that the present invention may be modified in numerous ways and may assume many embodiments other than that specifically set out and described above. For example, although the preferred embodiment that has been described provided a system clock and frequency lock signal to a processor as used in a data processing system, it will be appreciated that the present invention is applicable to other embodiments where other devices could utilize the frequency locked detection system of the present invention to be safely enabled for operation with the system clock. Further, while a dual bandwidth PLL has been described, a multiple bandwidth PLL could be used that operates in three or more selected bandwidths so that the bandwidth control signal produced by the frequency detector selects from the multiple bandwidths for the PLL operation. Accordingly, it is intended by the appended claims to cover all modifications of the invention which fall within the true scope of the invention.

L9: Entry 23 of 88 File: USPT Jun 2, 1992

DOCUMENT-IDENTIFIER: US 5119043 A
TITLE: Auto-centered phase-locked loop

CLAIMS:

18. A multi-frequency operating system having a phase-locked loop for controlling an output frequency of an oscillator and driving said output frequency to a selected one of a set of frequency bands, said loop comprising

circuitry for detecting phase and frequency errors between said oscillator output frequency and a reference frequency and producing a first error signal that represents said phase and frequency errors, said first error signal being equal to a reference level in the absence of said phase and frequency errors,

circuitry for generating a second error signal in response to low frequency differences between said first error signal and said reference level, said second error signal representing an average of said frequency errors, and

a controller for combining said first error signal and said second error signal to generate a drive signal and applying said drive signal to cause said oscillator to adjust said output to minimize said phase and frequency errors,

said controller including circuitry for scaling said second error signal in response to a change in the selected frequency band before said combining to correspondingly change a relative contribution of said second error signal with respect to said first error signal in said drive signal during changes in said selected frequency band.

L9: Entry 53 of 88 File: USPT Oct 21, 1980

DOCUMENT-IDENTIFIER: US 4229827 A
TITLE: Single voltage controlled oscillator modem

CLAIMS:

6. The modem of claim 5 wherein said phase locked loop means comprises a multichannel selector for selecting the channel over which said data is transmitted and received.

12. The modem of claim 11 wherein said phase locked loop means comprises a multichannel selector for selecting the channel over which said data is transmitted and received.

19. The modem of claim 18 wherein said phase locked loop means comprises a multichannel selector for selecting the channel over which said data is transmitted and received.

L9: Entry 15 of 88 File: USPT Jun 1, 1999

DOCUMENT-IDENTIFIER: US 5909149 A
TITLE: Multiband phase locked loop using a switched voltage controlled oscillator

Abstract Text (1):
A multi-band phase locked loop employing multiple, switchable voltage controlled oscillators. A single PLL is provided having a different voltage controlled oscillator for each desired frequency band of operation. The transfer function of the phase detector in the phase locked loop is switched responsive to the particular band selected so as to maintain the loop natural frequency at the same point regardless of other changes in the loop transfer function that are associated with operating at alternate frequencies, such as, but not limited to, changes in the frequency slope of the voltage controlled oscillators and changes in the division ratio of the loop divider circuit.

CLAIMS:

2. A multi-band phase locked loop as set forth in claim 1 wherein a transfer function of said voltage controlled oscillator is controlled relative to an overall transfer function of said phase locked loop so as to cause said phase locked loop to have approximately the same natural frequency regardless of the selected frequency band.

7. A multi-band phase locked loop as set forth in claim 6 wherein said transfer function of said phase detector is controlled relative to an overall transfer function of said loop so as to cause said loop to have approximately the same natural frequency regardless of the frequency band selected.

9. A multi-band phase locked loop as set forth in claim 7 wherein said phase detector has a gain that is programmable responsive said band select control signal.

12. A multi-band phase locked loop as set forth in claim 7 wherein said phase detector comprises at least first and second positive current sources and first and second negative current sources and wherein only said first current sources are enabled when said band select signal is in a first state and wherein said first and second current sources are enabled when said band select signal is in a second state.

L9: Entry 10 of 88 File: USPT Jul 18, 2000

DOCUMENT-IDENTIFIER: US 6091304 A
TITLE: Frequency band select phase lock loop device

Brief Summary Text (13):
To achieve these and other advantages and in accordance with the purpose of the present invention, as embodied and broadly described, a multi-band phase lock loop (PLL) device is provided, comprising a frequency reference oscillator for providing a frequency reference signal, a reference frequency divider for dividing the reference frequency, a phase and frequency detector for generating an output error signal based on frequency and phase information contained in the frequency reference signal and a second input frequency signal, a filter and compensation circuit for generating a fast and a slow feedback signal based on the error signal, a microcontroller for generating a frequency adjust signal and a band select signal based on the slow feedback signal and a band select input, a multi-band voltage controlled oscillator (VCO) for generating an output frequency signal based on the fast feedback signal, the frequency adjust signal and the band select signal, and a feedback divider for dividing the frequency of the signal generated by the multi-band VCO to provide the second input frequency signal for the phase and frequency detector. The frequency of the VCO output signal falls within one of a plurality of frequency bands depending on the band select signal. Within each frequency band, the VCO output frequency is controlled by the fast feedback signal, and frequency band centering is accomplished by the frequency adjust signal provided by the microcontroller.

Detailed Description Text (9):
The slow feedback signal 115 generated by the filter and compensation circuit 130 is preferably slower-varying than the fast feedback signal 111 for the phase lock loop. The slow feedback signal 115 is provided to the microcontroller 160, which also receives band select inputs 118 from an external source (not shown). Based on the slow feedback signal 115 and the band select input 118, the microcontroller 160 generates a band select signal 116 for frequency band selection and a frequency adjust signal 117 for frequency band centering of the multi-band VCO 140.

Detailed Description Text (10):
As illustrated in FIG. 2, the frequency of the VCO output signal 112 (the vertical axis) falls in a plurality of frequency bands such as Band 1, Band 2 and Band 3. These frequency bands may be disconnected (i.e. non-overlapping) bands. For example, one frequency band may be a band used by analog cellular phones (the 800 MHz band) and another band may be a band used by PCS (the 1900 MHz band). Alternatively, the bands may partially overlap (not shown) to provide phase lock operation over a single band covering a larger frequency range than any individual band. The band select signal 116 from the microcontroller 160 determines which frequency band the output signal 112 of the VCO 140 falls in. Within each frequency band, the frequency of the output signal 112 varies with the size of the fast feedback signal 111 (the horizontal axis) as indicated by the dashed lines 21a, 21b and 21c. For example, within Band 2, the VCO output frequency varies from F21 to F22 as the fast feedback signal 111 increases from V21 to V22. The phase lock loop formed by the phase and frequency detector 120, the filter and compensation circuit 130, the multi-band VCO 140 and the feedback divider 150 operates to lock the frequency of the VCO output signal 112 to a frequency within one of the frequency bands. Thus, by using the multi-band VCO 140, the frequency of the output signal 112 may be locked to an expanded range of frequencies. A precise frequency may be generated at each frequency band for use in a communication device, for example, as a local oscillator for down converting a received signal in a communication receiver.

Detailed Description Text (35):
FIG. 8 illustrates a multi-band VCO 140 and logic 160a suitable for use in the phase lock loop of FIG. 7. This embodiment has a simplified structure including a two-band VCO 140 having a single parallel band select circuit, and logic 160a having two inverters (G81 and G82) for band select operation. The two frequency bands may be, for example, the analog cellular band (800 MHz) and the PCS band (1900 MHz), respectively. This structure provides no frequency band centering capabilities; instead, tolerance control, and main varactor tuning (of VC81 and VC82) are used to provide multi-band frequency control. This simplified structure reduces the number of components, power consumption, size, and cost of the communication devices in which it is applied.